**Why Design for Test (DFT) and Where It Goes**

With increasing complexity and size of integrated circuits, today’s large SoCs are more and more difficult to test and verify. It is not only very expensive but also extremely time consuming. This challenge is going to stay with Moore’s law continuing to take effect. IC companies are putting more and more resources to tackle these problems. The goal is to ensure fast time-to-market, high product quality, low test cost, and quick yield ramp-up.

In order to achieve this goal, at the early stage of architectural design testing has to be taken into account. The effect of DFT goes through the entire design flow but it does not stop there. This presentation will review some of important roles that DFT plays in post-silicon verification/debug, manufacture test and yield analysis. Hopefully this talk can serve as a starting point for discussion that we could learn and benefit from each other.

**BIO**

Liyang Lai is a member of Consulting Staff at Calypto Design Systems, a company owned by Mentor Graphics. He obtained his Ph.D. in Electrical Engineering from University of Illinois at Urbana Champaign in 2005, M.S. in Institute of Microelectronics in Chinese Academy of Sciences in 2000, and B.S. in Peking University in 1997.

He has been with Mentor Graphics, a world leader in DFT solutions, since 2005. His research interests include DFT, verification, fault diagnosis and SoC design. He has over ten years industrial experience in VLSI testing, from front end (design) to back end (diagnosis), and to yield learning. As a key member in Mentor’s Design for Test group, the products that he made critical contributions have won a number of industrial awards, including 2013 DesignCon IC Design Tools Award, 2009 Test & Measurement World Test-of-Time Award. Many solutions he proposed and implemented have been adopted by semiconductor companies worldwide (such as INTEL, AMD, BroadCom etc).

He is an inventor of multiple patents on DFT and diagnosis, a member of the IEEE, a working group member on STDF Memory Fail Datalog, and reviewer for many conferences and journals. He has published a number of papers on world renowned conferences and journals in design for test, and is best paper award winner of 2006 International Test Conference.

赖李洋是美国Calypto Design Systems 公司研究员。他1997年毕业于北京大学计算机系微电子学专业，2000年获中科院微电子所硕士学位。2005年获美国University of Illinois at Urbana-Champaign（UIUC）电子工程博士学位，师从于国际著名计算机体系结构和VLSI测试专家Professor Janak H. Patel。

博士毕业后一直在美国Mentor Graphics公司工作。Mentor是世界第一的可测性设计解决方案提供商。他主要从事集成电路可测试性设计，验证，故障诊断的研究。拥有完整的VLSI测试从前端到后端，以及芯片良率分析的业界经验。做为核心研发人员，他研发的芯片可测性设计产品，获得了多个产业界的重要奖项，包括2013 DesignCon IC Design Tools Award, 2009 Test & Measurement World Test-of-Time Award。他所提出和实现的可测性设计解决方案已经为世界许多半导体公司所采用（比如INTEL，AMD，BroadCom等）。

他是多项可测试性设计及故障诊断专利的发明人，IEEE Member，STDF Memory Fail Datalog标准委员会成员和多项国际会议及期刊如ITC，VTS，ICCAD的审稿人。在本研究领域顶级国际会议和期刊发表多篇学术论文，并获得2006 年International Test Conference最佳论文奖。